Docket No.: 061282-0048 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Shinya TOKUNAGA, et al.	:	Confirmation Number: 4744
Application No.: 10/722,346	:	Group Art Unit: 2825
Filed: November 26, 2003	:	Examiner: SIEK, VUTHE

For: MASK PATTERN INSPECTING METHOD, INSPECTION APPARATUS, INSPECTING DATA USED THEREIN AND INSPECTING DATA GENERATING METHOD

TRANSMITTAL OF CERTIFIED TRANSLATION OF PRIORITY DOCUMENT

Mail Stop Priority Document
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In furtherance of the response filed on November 16, 2005, enclosed please find a certified translation of Priority Document, Japanese Patent Application No. HEI 2002-342304, filed November 26, 2002.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

for #46,692

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Date: February 6, 2006

PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Shinya Tokunaga etal.
Appln. No.: 10/722,346 Group Art Unit:
Filed: November 26, 2003 Examiner:
For: Mask Pattern Checking Method, Checking Apparatus, Checking Data Used Therein and Checking Data Generating Method

STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir/Madam:

I, Satoshi Watanabe, of Ark Mori Building, 13F, 12-32, Akasaka 1-chome, Minato-ku, Tokyo 107-6028, Japan, hereby state that:

I well understand the Japanese and English languages and attached is an accurate English translation made by me of the Japanese specification in the above-identified U.S. patent application.

Date : February 1, 2006 Name : Satoshi WATANABE

PATENT OFFICE

Japanese Government

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: November 26, 2002

Application Number: Japanese Patent Application No. Hei. 2002-342304

Applicant(s): Matsushita Electric Industry Co., Ltd.

Commissioner,
Patent Office:

(Seal)

Issuance No.

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[Filing date] December 1, 2000

[Indication of Fee]
[Registered Number of the Prepayment] 092740
[Amount of Payment] 21000

[List of Filed Documents]
[Filed Document Name] Specification 1
[Filed Document Name] Drawing 1
[Filed Document Name] Abstract 1
[Number of General Power] 0002926

[Request for Proof] Request

[Designation of Document] Specification

[Title of the Invention] Mask Pattern Checking Method, Checking Apparatus, Checking Data Used Therein and Checking Data Generating Method

[Claims]

[Claim 1] A method of checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising the steps of:

classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting the same;

determining checking precision for each of the ranks; and

deciding quality of the photomask depending on whether the determined checking precision is satisfied for each drawing pattern thus extracted.

[Claim 2] The method of checking a photomask according to claim 1, wherein the reference is a functional feature of the drawing pattern, and

the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same depending on the functional feature of the drawing pattern.

[Claim 3] The method of checking a photomask according to claim 2, wherein the extracting step serves to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern is a dummy pattern.

[Claim 4] The method of checking a photomask according to claim 2, wherein the extracting step serves to classify the drawing pattern in the chip region of the semiconductor integrated circuit into a plurality of ranks and to extract the same depending on whether the drawing pattern has the same node.

[Claim 5] The method of checking a photomask according to any of claims 1 to 4, wherein the reference is a feature of a shape of the drawing pattern, and

the extracting step serves to classify the drawing pattern

into a plurality of ranks and to extract the same depending on the feature of the shape of the drawing pattern.

[Claim 6] The method of checking a photomask according to claim 5, wherein the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same based on a distance from the closest pattern.

[Claim 7] The method of checking a photomask according to claim 5, wherein the extracting step serves to classify the drawing pattern into a plurality of ranks and to extract the same based on a distance from a corner of the drawing pattern.

[Claim 8] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each pattern.

[Claim 9] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each line (pattern edge).

[Claim 10] The method of checking a photomask according to any of claims 1 to 7, wherein the extracting step serves to classify the drawing pattern into the ranks and to extract the same depending on the reference for each area.

[Claim 11] The method of checking a photomask according to any of claims 1 to 9, wherein the deciding step serves to change a precision condition depending on an increase or decrease in a pattern width.

[Claim 12] The method of checking a photomask according to any of claims 1 to 11, wherein the deciding step serves to detect whether the drawing pattern is a dummy pattern and to relax the precision condition when the drawing pattern is the dummy pattern.

[Claim 13] The method of checking a photomask according to any of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node and to relax the precision condition when they have the same node.

[Claim 14] The method of checking a photomask according to any

of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node based on a pattern in the same layer and to relax the precision condition when they have the same node.

[Claim 15] The method of checking a photomask according to any of claims 1 to 12, wherein the deciding step serves to detect whether at least two patterns have the same node by a contact through a pattern in a layer positioned on or under the layer, and to relax the precision condition when they have the same node.

[Claim 16] The method of checking a photomask according to any of claims 1 to 12, wherein when the drawing pattern is a wiring pattern including a contact array,

the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken.

[Claim 17] The method of checking a photomask according to any of claims 1 to 12, wherein when the drawing pattern is a pattern for forming a contact hole,

the deciding step serves to detect whether one contact array or more is/are taken and to change the precision condition depending on whether one contact array or more is/are taken.

[Claim 18] The method of checking a photomask according to claim 1, wherein the extracting step serves to classify the drawing pattern into two ranks and to extract the same depending on whether a critical point determined by an intersection of a relational expression of a manufacturing defect density and a manufacturing defect size in a photomask and a relational expression of a pattern area weighed by a manufacturing defect generation probability on a pattern and the manufacturing defect size is exceeded based on the critical point.

[Claim 19] An apparatus for checking a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising:

means for classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks

in accordance with a predetermined reference and extracting a plurality of pattern data;

means for determining checking precision which is required for each of the ranks and generating precision data; and

means for deciding whether the pattern data satisfy the precision data for each of the classified pattern data.

[Claim 20] Checking data of a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising:

a plurality of pattern data extracted by a classification of a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference; and

precision data indicative of checking precision which is required for each of the ranks.

[Claim 21] A method of generating checking data of a photomask for a semiconductor integrated circuit formed based on drawing pattern data, comprising the steps of:

classifying a drawing pattern in a chip region of the semiconductor integrated circuit into a plurality of ranks in accordance with a predetermined reference and extracting a plurality of pattern data; and

determining checking precision which is required for each of the ranks and generating precision data.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs]

The present invention relates to a method of checking a mask pattern, a checking apparatus, checking data used therein and a method of generating the checking data, and more particularly to the extraction and check of checking precision data in a process for checking a photomask.

[0002]

[Prior Art]

In recent years, a semiconductor integrated circuit device (hereinafter referred to as an LSI) in each product is evaluated

as a key device, and an increase in the scale and speed of the LSI has been required in order to maintain the competitiveness of the product. A fine process is necessary with the microfabrication of an element and an increase in integration.

Under the circumstances, process conditions have been increasingly restricted in order to form a pattern as designed.

[0003]

In the formation of the semiconductor integrated circuit device, an isolation is carried out over the surface of a semiconductor substrate and a well having a desirable concentration is formed, and an impurity diffusion region having a desirable conductivity type is formed in the well, and furthermore, an insulating film is formed and a wiring pattern is provided.

[0004]

For example, in the formation of the wiring pattern, a photolithographic step of forming a conductive film such as a polycrystalline silicon layer, an aluminum layer or a metal silicide layer and then carrying out exposure through a photomask to form a desirable mask pattern is carried out, and etching is performed by using the mask pattern as a mask, thereby forming the wiring pattern.

[0005]

At the etching step, the conductive film exposed from the mask pattern is selectively removed. Even if various conditions such as the concentration and temperature of an etchant are optimized, an etching speed is varied depending on the density (area ratio) of the mask pattern, and furthermore, the peripheral length of the mask pattern. For this reason, precision in etching is varied depending on the density of the mask pattern or a pattern pitch. Even if a mask pattern region is excessively large or small, the precision in the etching is reduced.

[0006]

Moreover, the formation of a diffusion layer also has the same problems. If an ion implantation region for forming the diffusion layer is too small, the concentration of the ion is

generated so that a desirable diffusion profile cannot be obtained. Accordingly, the precision in the photomask for forming the mask pattern for diffusion is also very important.
[0007]

In each process, a pattern is formed by using the photomask. The pattern precision of the mask pattern on the photomask greatly depends on the precision in the pattern formation in the process. Therefore, a demand for an enhancement in the precision has been increased.
[0008]

Under the circumstances, at a defect checking step, necessary precision for a region which is to have the highest precision in a photomask to be checked is acquired from a photomask designer and a check is carried out by using a value thereof as a reference value. Thus, an effort to reduce the defect of the photomask has been made.
[0009]

For this reason, over one photomask, all regions are checked based on the same check reference. Therefore, a defect set within such a range as not to originally influence an actual circuit operation is treated to be present, and correction or manufacture is carried out again. Consequently, there is a problem in that a time (TAT) required from an order to a completion is increased.

Moreover, the photomask is expensive. Therefore, a sudden rise in a cost caused by the necessity of a large number of photomask blanks for carrying out the manufacture again is also a serious problem.
[0010]

In a recent process for manufacturing a semiconductor integrated circuit, moreover, there has been proposed a method of CMP (Chemical Mechanical Etching) for flattening the surface of a substrate. For example, this method serves to form an insulating film on a surface by a coating method of a CVD method and to then carry out chemical etching while performing mechanical polishing, thereby flattening the surface. In the

case in which the pattern density of a wiring layer to be a lower layer is low and there is a region including a pattern having a predetermined area or less, however, the flattening cannot be carried out even if the insulating film is formed thickly. As a result, a region having no wiring pattern after the CMP becomes a concave portion so that a dent state is maintained.
[0011]

In the case in which the layout pattern has a deviation, thus, sufficient pattern precision for the layer cannot be obtained. In addition, there is a problem in that the pattern precision of an upper layer is also influenced. Consequently, there is a problem in that the process precision cannot be sufficiently obtained.
[0012]

Therefore, the applicant has proposed a method of extracting the area ratio of the mask pattern from the layout pattern of a semiconductor chip, additionally providing a dummy pattern to the layout pattern to adapt the area ratio of the mask pattern of a layer constituting the layout pattern in consideration of the optimum area ratio of the layout pattern of the layer obtained based on the process conditions of the layer, thereby setting the layer to have the optimum area ratio (see Patent Document 1).
[0013]

[Patent Document 1]

JP-A-2002-229215
[0014]

A photomask to be a very important element in such an increase in precision in a pattern is used through a defect checking step.

Also in the check, necessary precision in a portion in which the toughest precision conditions in the photomask to be checked is acquired from the designer of the photomask and the check is carried out by using the data.

According to this method, it is possible to advance the check without specifying a place having the toughest portion

in the creation and check of the photomask. Thus, a yield can be enhanced.

[0015]

Description will be given to a conventional photomask checking flow with reference to the drawings.

Fig. 20 is a flow chart showing a conventional photomask check.

In this method, first of all, the pattern of a photomask is created based on a design rule (step 101). Next, the pattern of the photomask thus obtained is converted into data for photomask drawing and data are transferred to the manufacturing division of the photomask or another manufacturing company thereof so that a photomask is started to be actually manufactured (step 102).

[0016]

The minimum value of the design rule of a pattern is specified as check precision data when the data are thus transferred (step 106).

On the other hand, the photomask manufacturing division or another manufacturing company thereof draws a pattern on a photomask blank by using the drawing data of the photomask formed at the step 102, thereby forming the photomask (step 103).

Next, the result of the pattern formation is decided based on the checking precision data obtained at the step 106 (step 104).

Then, it is decided that only the pattern formation decided to be within the range of the checking precision data is acceptable.

[0017]

With the recent microfabrication of a process, however, a minimum pattern width and a minimum interval tend to be increasingly reduced. For example, consideration will be given to the case in which there is formed a photomask including patterns 210 to 213 having a minimum width which is arranged at a minimum interval 203 as shown in Fig. 21(a) and patterns 214 to 216 provided at a large interval 204 as shown in Fig. 21(b). For example,

it is assumed that the tolerance of a defect formed in a pattern having the minimum interval 203 is set to have a size represented by an allowable defect 201. At this time, in the case in which a pattern defect 206 having a smaller size than the size of the defect 201, it is decided that this is the tolerance at the checking step.

[0018]

In the case in which there is a pattern defect 202 having a greater size than the size of the allowable defect 201, moreover, it is decided that the photomask is a defect in the check because the defect 202 is larger than the allowable defect 201 at the checking step.

However, the allowable defect 201 has one size in the same photomask and the same processing is carried out based on the allowable defect 201 in any region having a great pattern width.

[0019]

[Problems that the Invention is to Solve]

For this reason, in the case in which there is the pattern defect 202 having a greater size than the size of the allowable defect 201, the interval 204 is much greater than the minimum interval 203 as shown in Fig. 21(b). Therefore, it is decided that the defect 202 is also a defect at the checking step between the patterns 214 and 215. Even if such a defect is thus present in the region having a great interval in an actual design rule, however, there is no problem. In spite of the foregoing, a correcting step is started so that a step of carrying out a check again is added.

[0020]

In the conventional method, thus, a demand for checking precision corresponding to the minimum interval 203 is given over the whole photomask. Therefore, it is decided that the defect 202 having such a size as not to make troubles is also a defect at the checking step.

[0021]

Also in the case in which the same defect is generated and patterns might be actually short-circuited with each other,

there is no problem when an adjacent pattern has the same node or a dummy pattern is formed for the purpose. Accordingly, it is not necessary to carry out the correction. However, the same defect is decided to be a defect in this case, the correcting step is started and the step of carrying out the check again is added.

Therefore, the check is executed with unnecessary precision so that a correction frequency is increased. Consequently, there is an obvious problem in that a reduction in a photomask creating period (TAT) and a decrease in the cost of creation are hindered.

[0022]

In consideration of the actual circumstances, the invention has been made and has an object to provide a method of checking a photomask which can shorten a TAT and decrease a cost.

It is another object to provide an apparatus for checking a photomask which can shorten the TAT and decrease the cost.

It is yet another object to provide checking data capable of shortening the TAT and decreasing the cost in order to create the photomask.

It is a further object to provide a method of generating checking data which can shorten the TAT and decrease the cost in order to create the photomask.

[0023]

[Means for Solving the Problems]

In order to attain the objects, a method according to the invention is characterized in that precision data on each pattern are extracted based on the feature of the pattern of a chip region and a check is carried out based on the precision data so that the check can be performed with high precision.

The chip region of a semiconductor integrated circuit indicates a functional region excluding the scribe line of a semiconductor chip.

[0024]

More specifically, the invention provides a method of

FIG. 9A

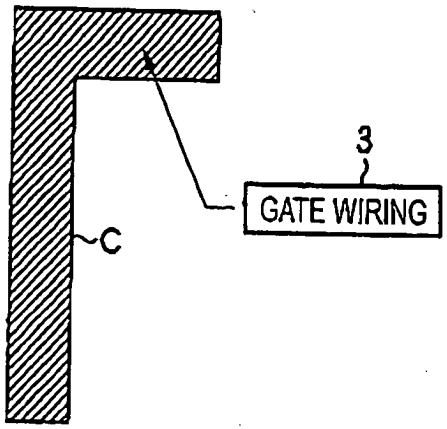


FIG. 9B

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION

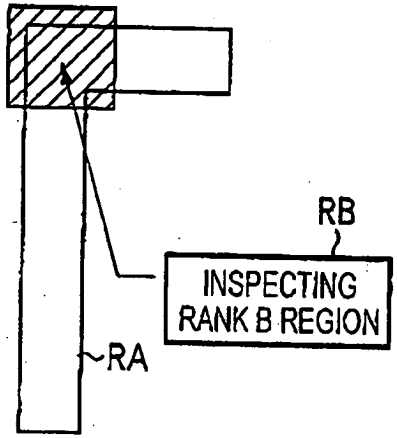


FIG. 9C

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

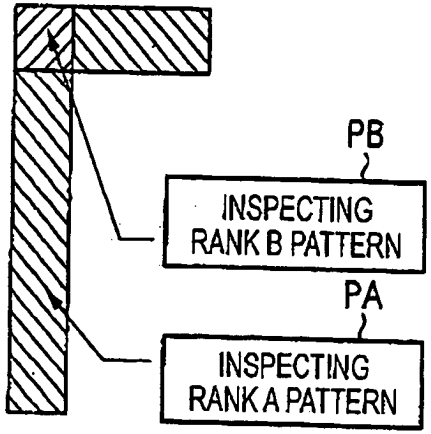


FIG. 9D

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

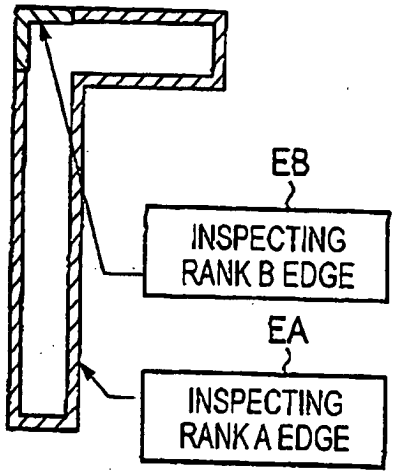


FIG. 10

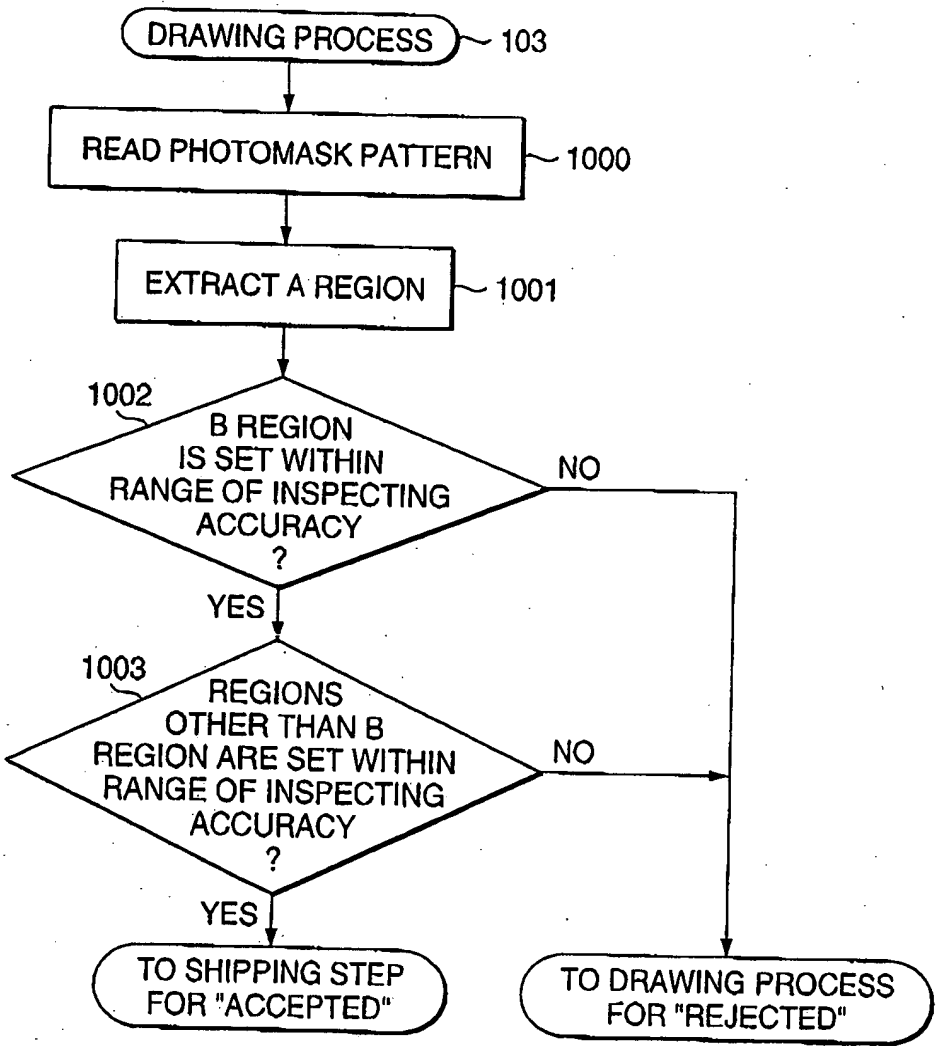

DRAWING PROCESS
103
READ PHOTOMASK PATTERN
1000
EXTRACT A REGION
1001
1002
B REGION IS SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
1003
REGIONS OTHER THAN B REGION ARE SET WITHIN RANGE OF INSPECTING ACCURACY ?
NO
YES
TO SHIPPING STEP FOR "ACCEPTED"
TO DRAWING PROCESS FOR "REJECTED"

FIG. 11A

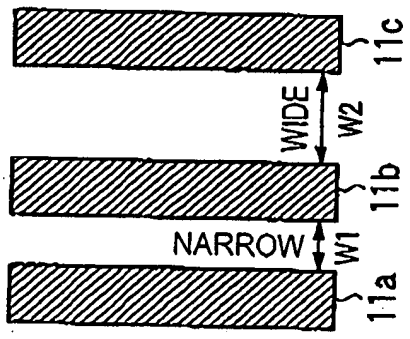


FIG. 11B

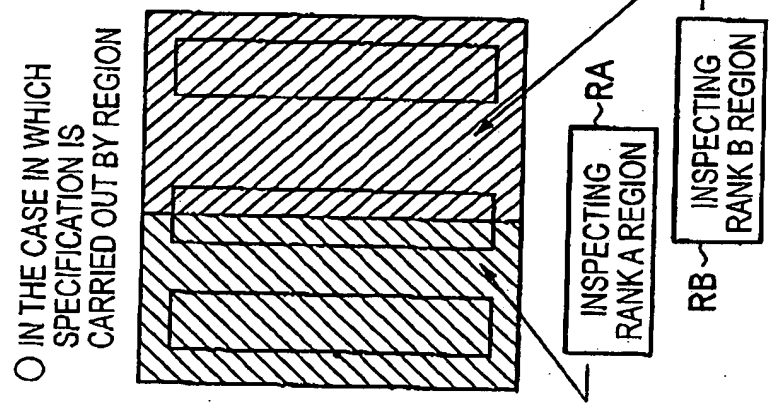


FIG. 11C

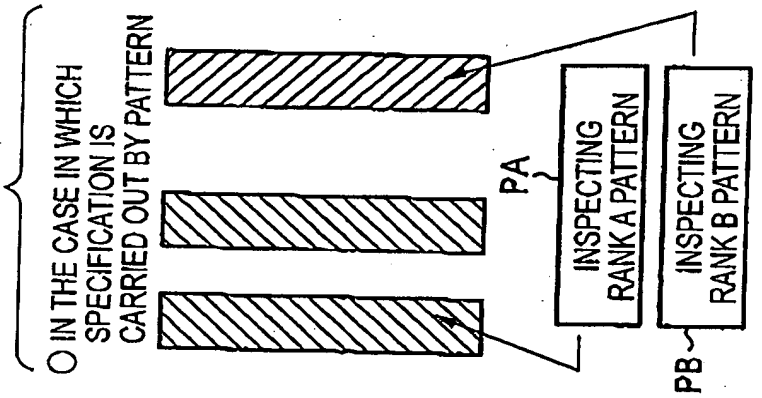


FIG. 11D

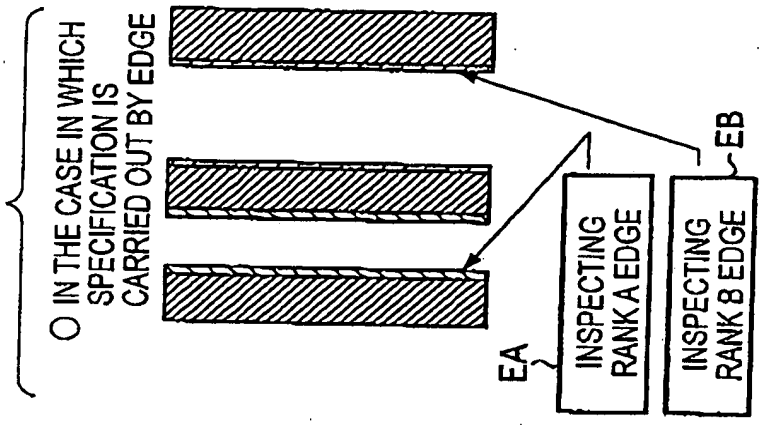


FIG. 12A

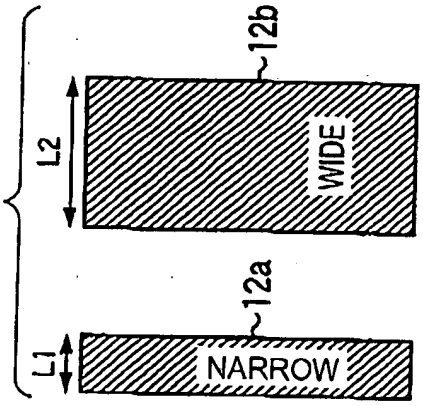


FIG. 12B

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY REGION

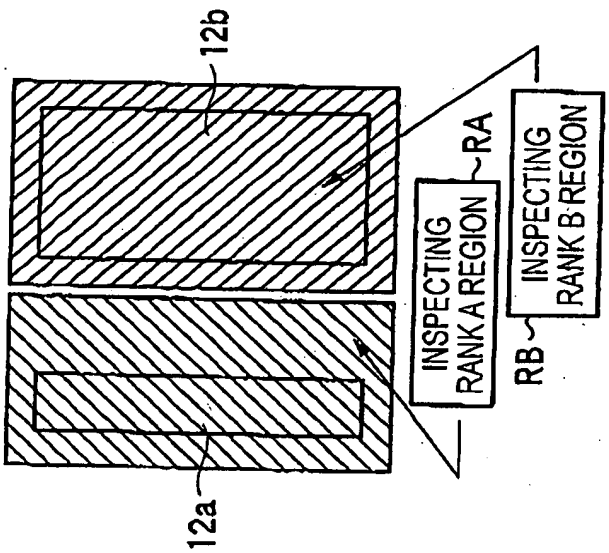


FIG. 12C

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY PATTERN

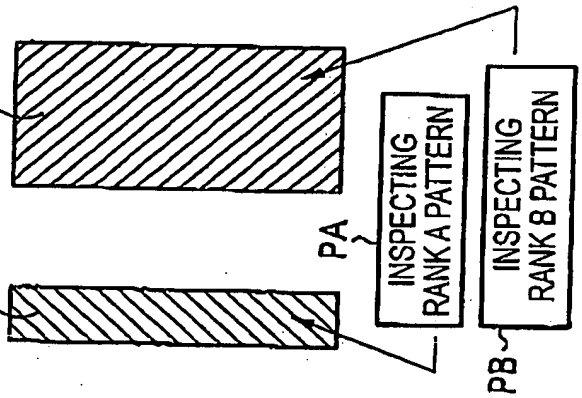


FIG. 12D

○ IN THE CASE IN WHICH SPECIFICATION IS CARRIED OUT BY EDGE

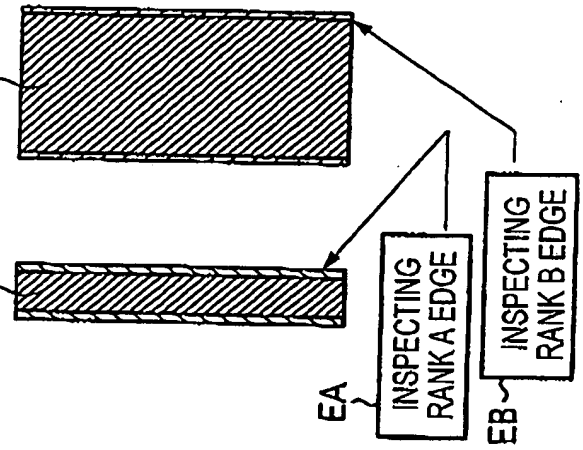


FIG. 13A

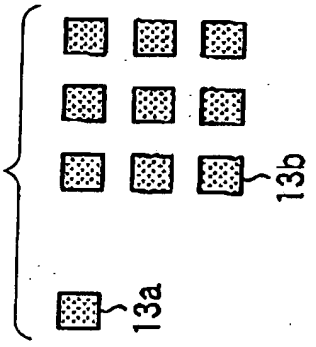


FIG. 13B

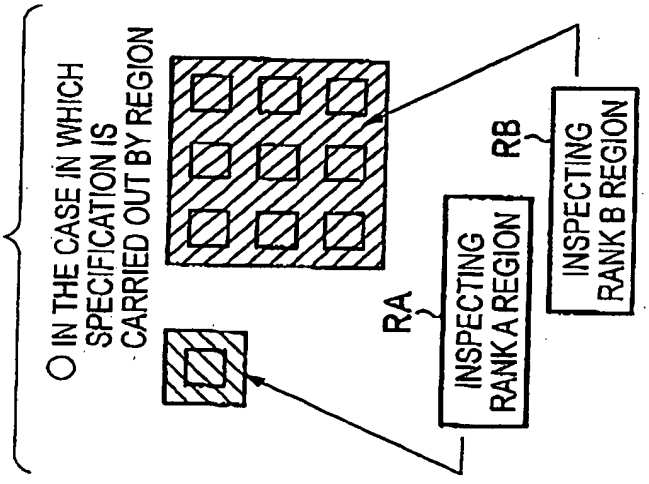


FIG. 13C

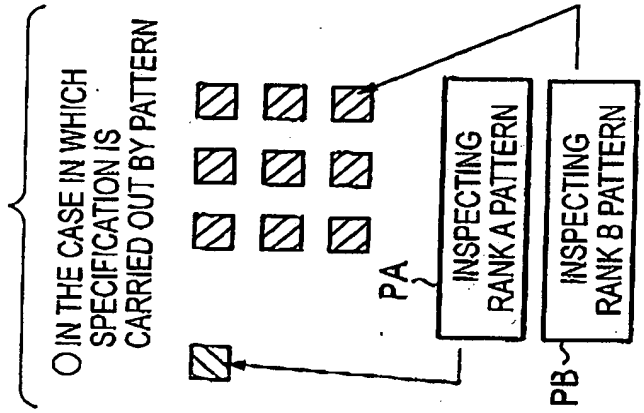


FIG. 13D

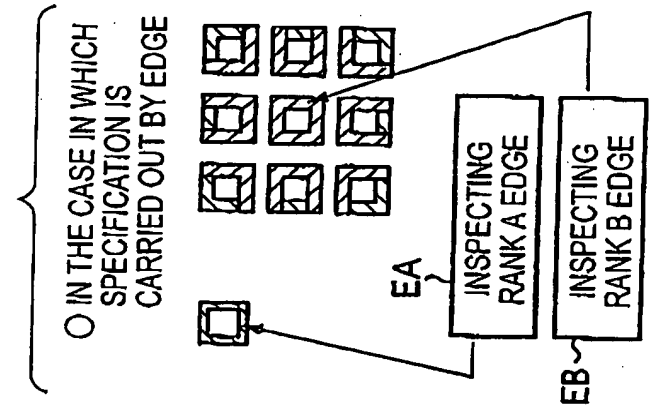


FIG. 14A

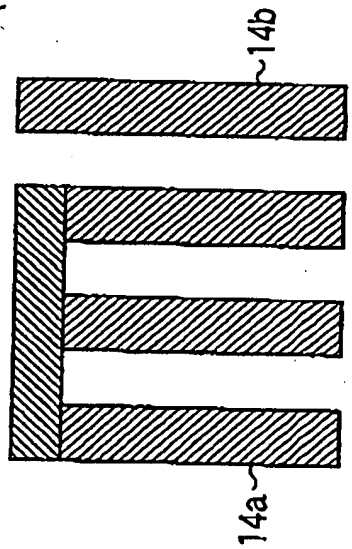


FIG. 14B

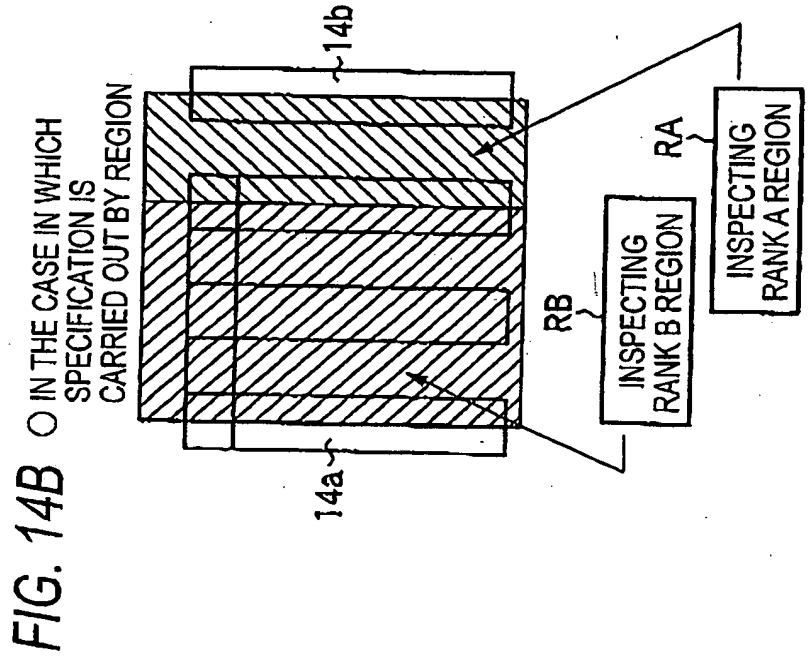


FIG. 14C

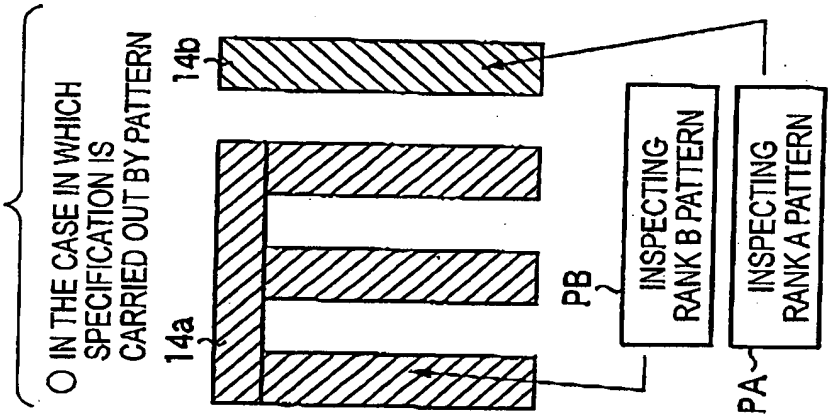


FIG. 14D

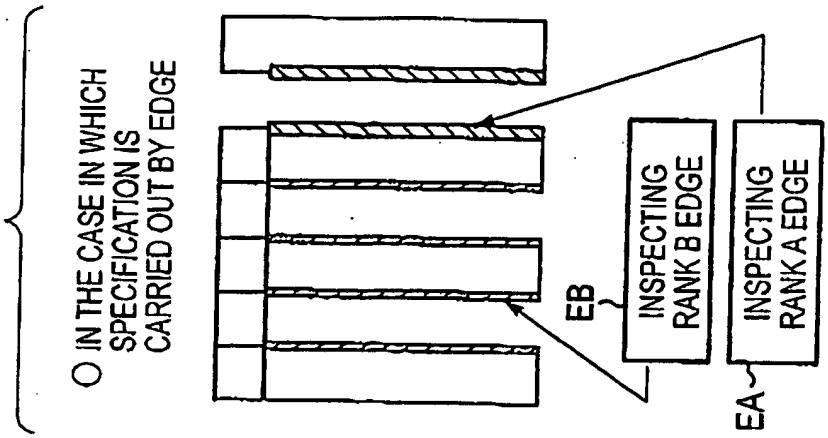


FIG. 15

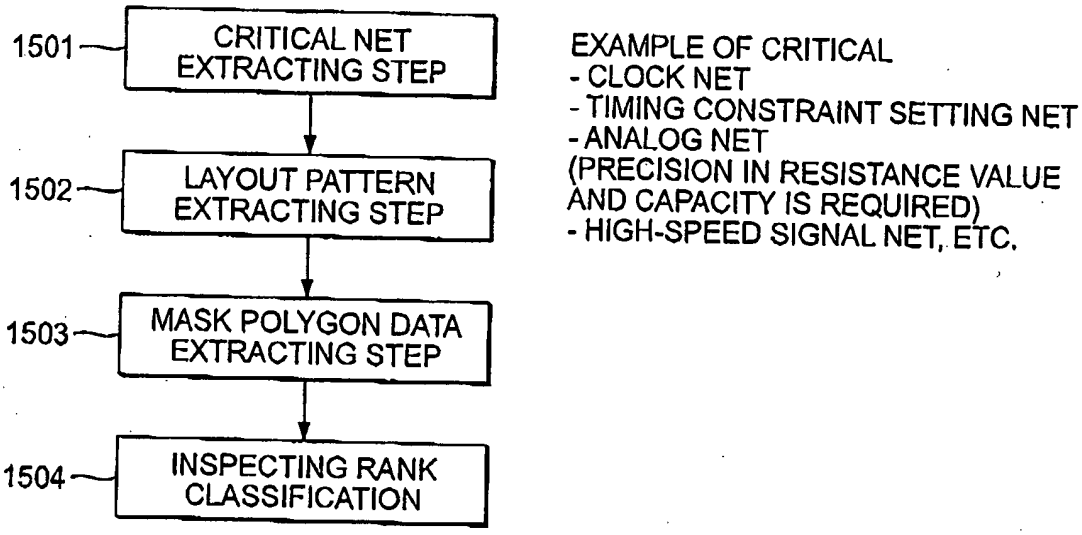

1501
CRITICAL NET EXTRACTING STEP
1502
LAYOUT PATTERN EXTRACTING STEP
1503
MASK POLYGON DATA EXTRACTING STEP
1504
INSPECTING RANK CLASSIFICATION
EXAMPLE OF CRITICAL
- CLOCK NET
- TIMING CONSTRAINT SETTING NET
- ANALOG NET
(PRECISION IN RESISTANCE VALUE AND CAPACITY IS REQUIRED)
- HIGH-SPEED SIGNAL NET, ETC.

FIG. 16

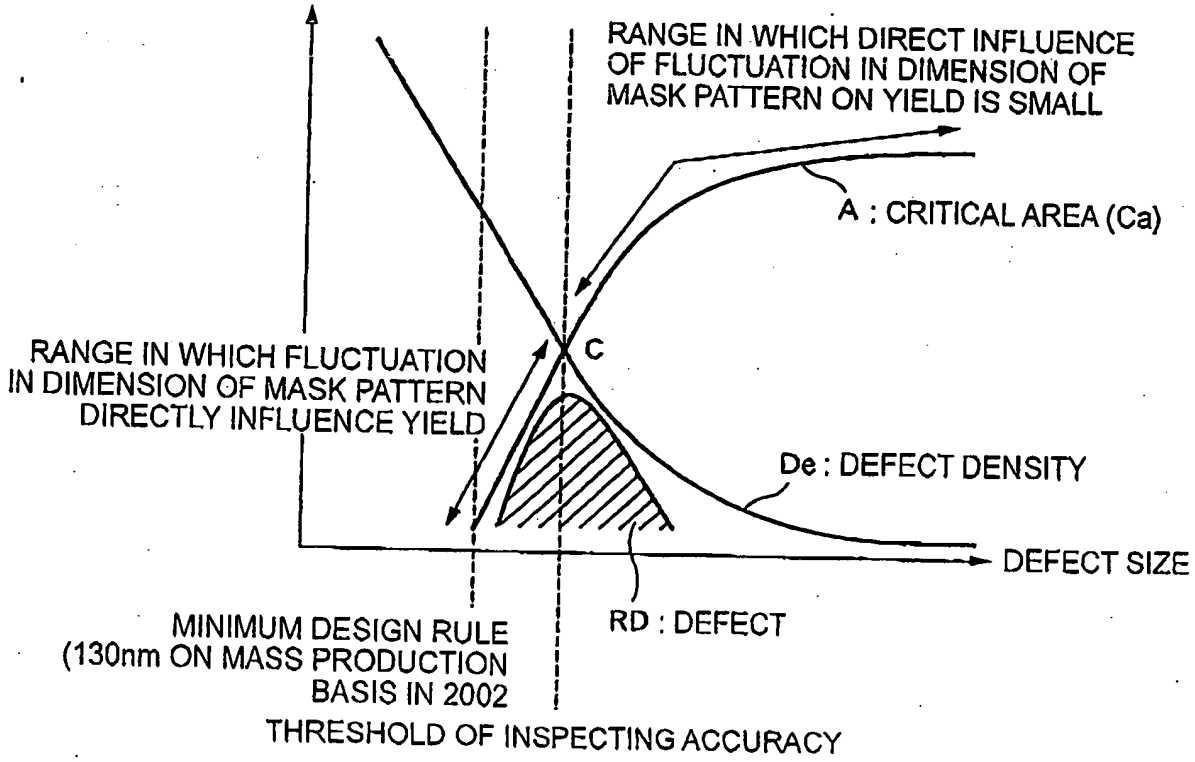

RANGE IN WHICH DIRECT INFLUENCE OF FLUCTUATION IN DIMENSION OF MASK PATTERN ON YIELD IS SMALL
A : CRITICAL AREA (Ca)
C
RANGE IN WHICH FLUCTUATION IN DIMENSION OF MASK PATTERN DIRECTLY INFLUENCE YIELD
De : DEFECT DENSITY
DEFECT SIZE
RD : DEFECT
MINIMUM DESIGN RULE (130nm ON MASS PRODUCTION BASIS IN 2002
THRESHOLD OF INSPECTING ACCURACY

FIG. 17A

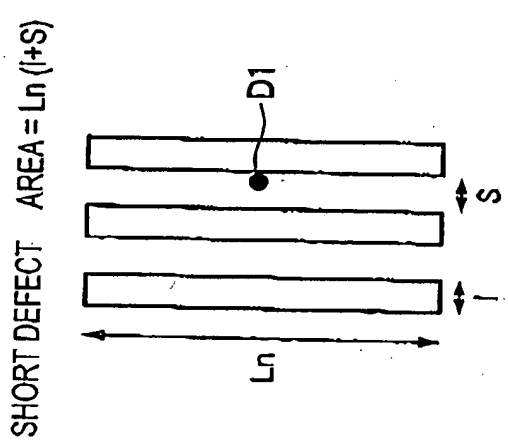


FIG. 17B

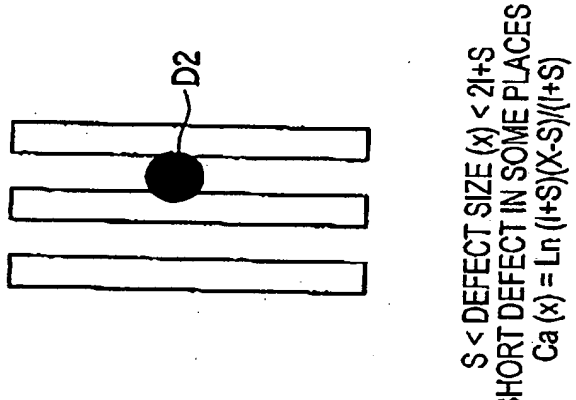


FIG. 17C

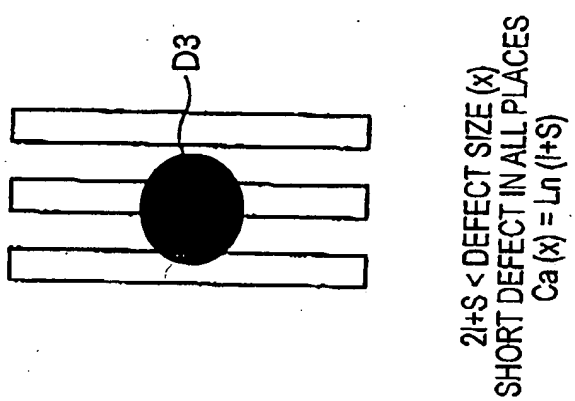


FIG. 18A

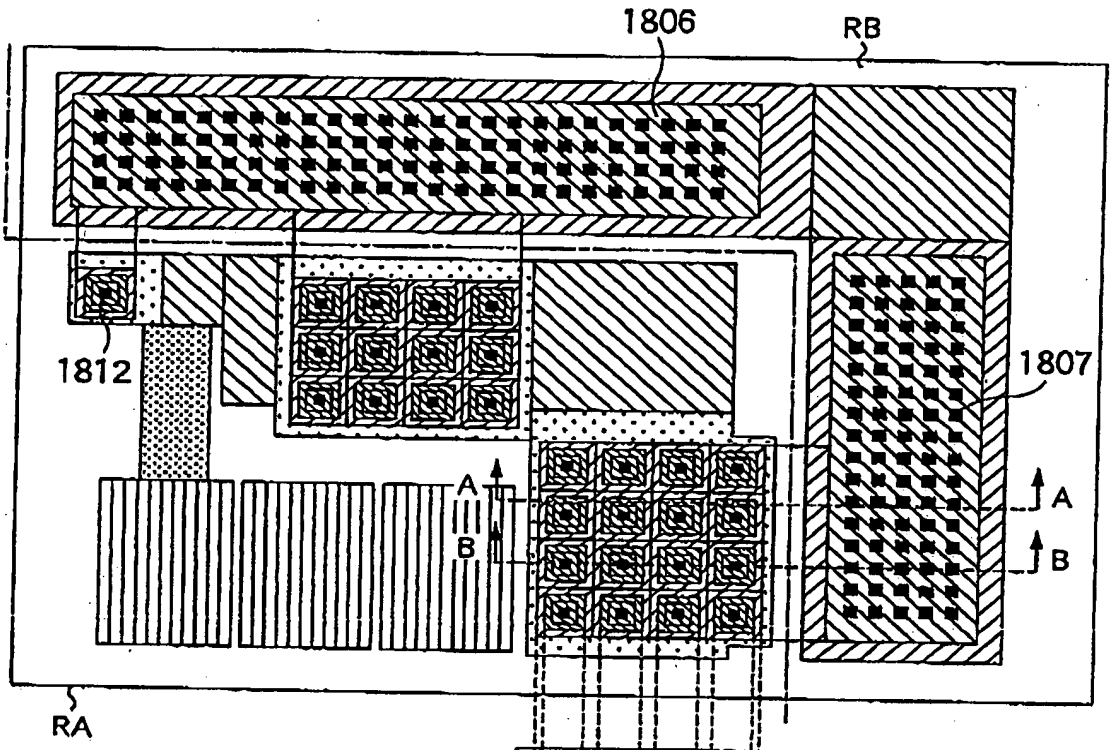


FIG. 18B A-A

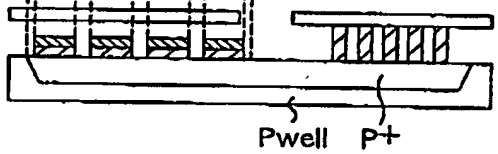
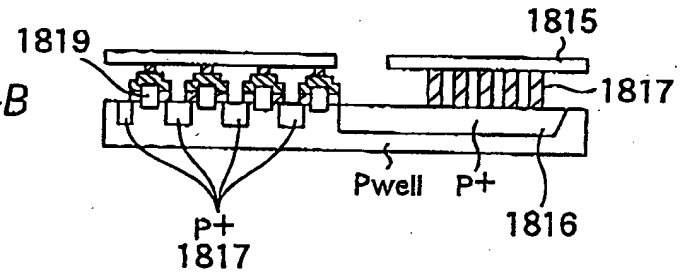


FIG. 18C B-B



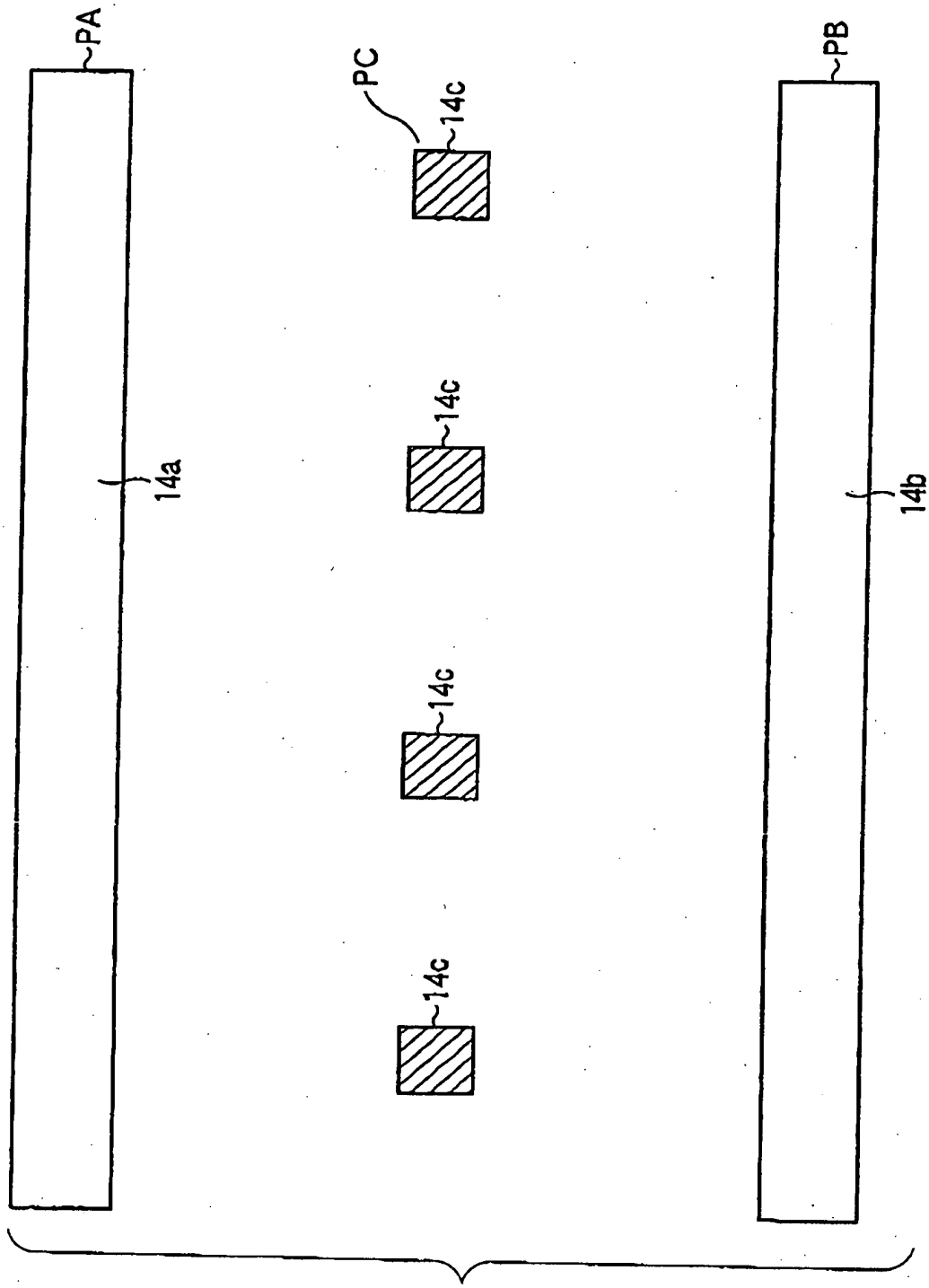


FIG. 19

FIG. 20

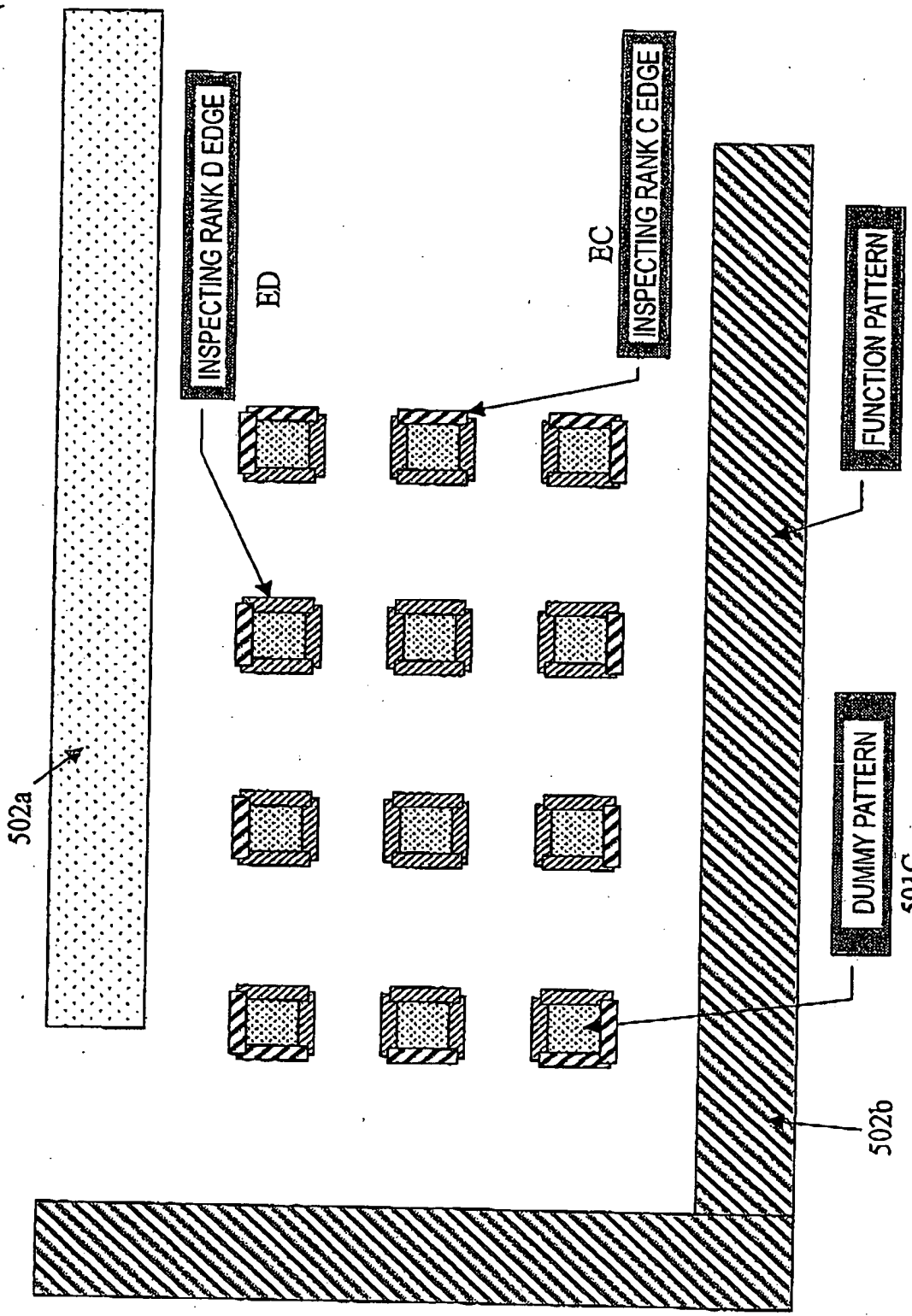

INSPECTING RANK D EDGE
ED
EC
INSPECTING RANK C EDGE
FUNCTION PATTERN
502a
DUMMY PATTERN
501C
502b

FIG. 21

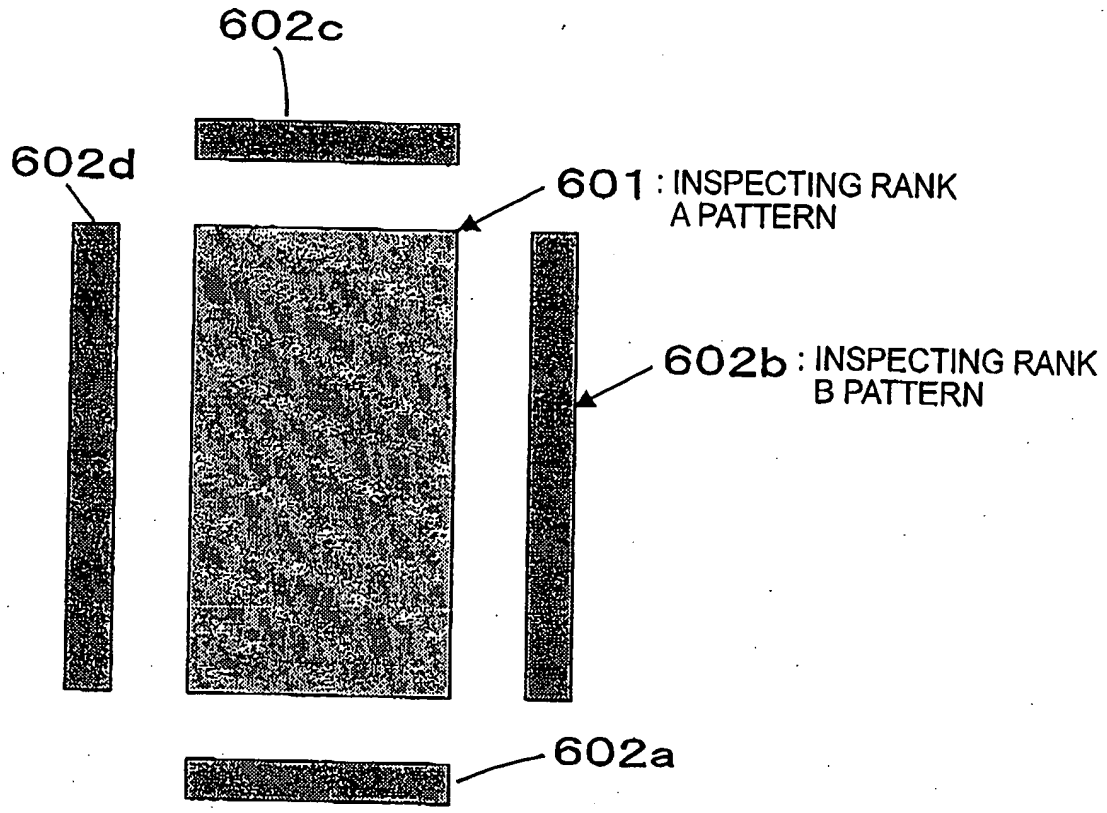

602c
602d
601 : INSPECTING RANK A PATTERN
602b : INSPECTING RANK B PATTERN
602a

FIG. 22

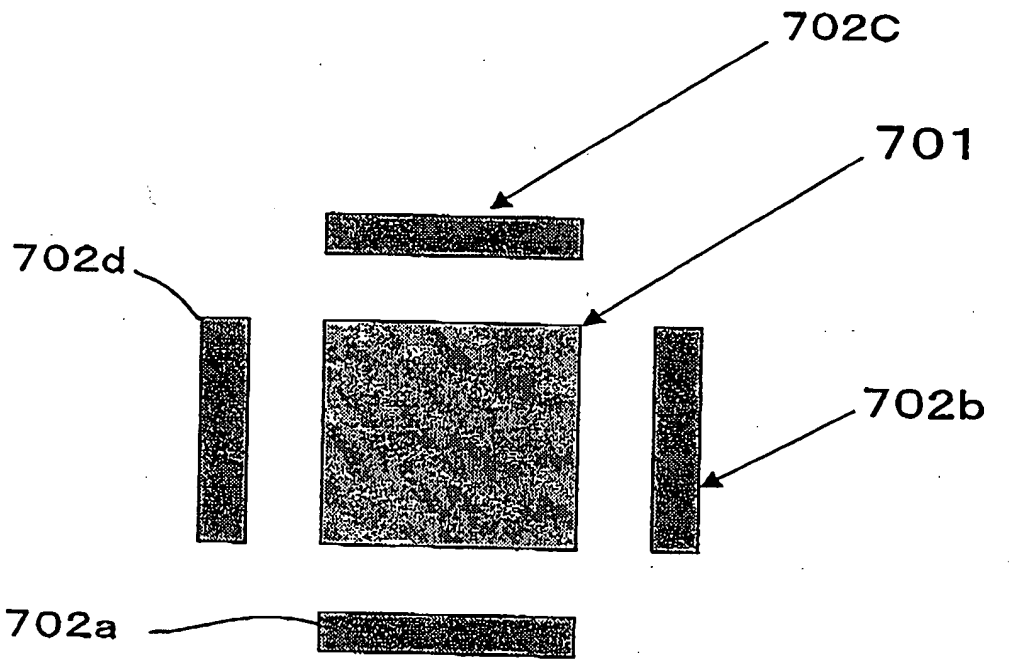


FIG. 23

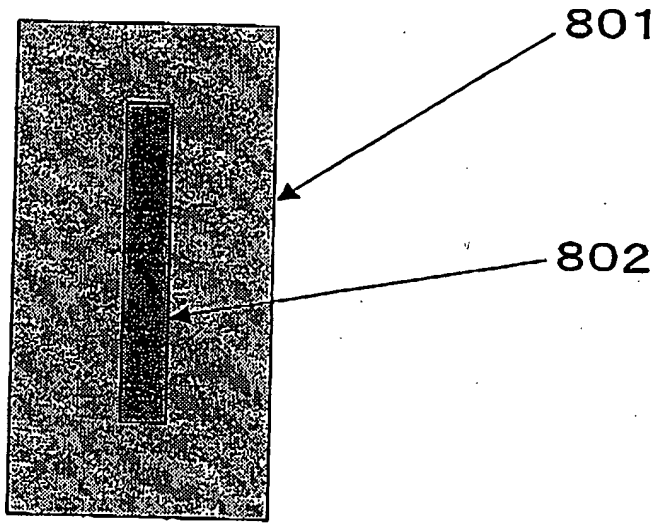


FIG. 24A

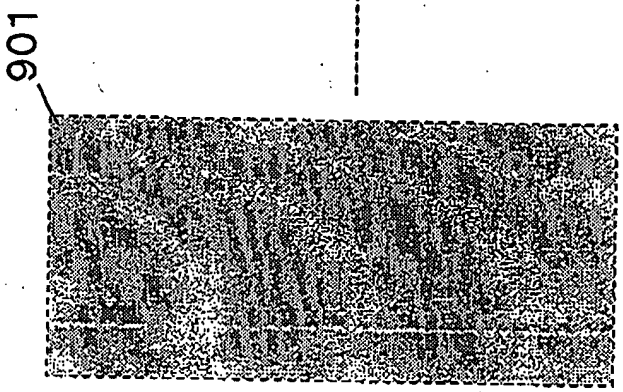


FIG. 24B

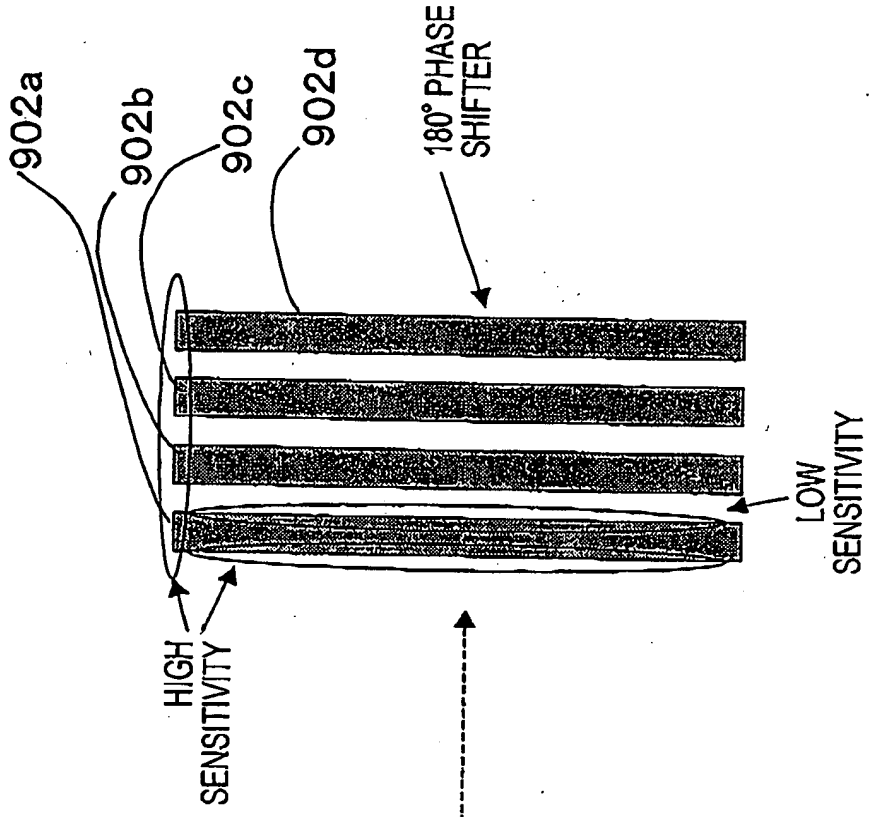


FIG. 25

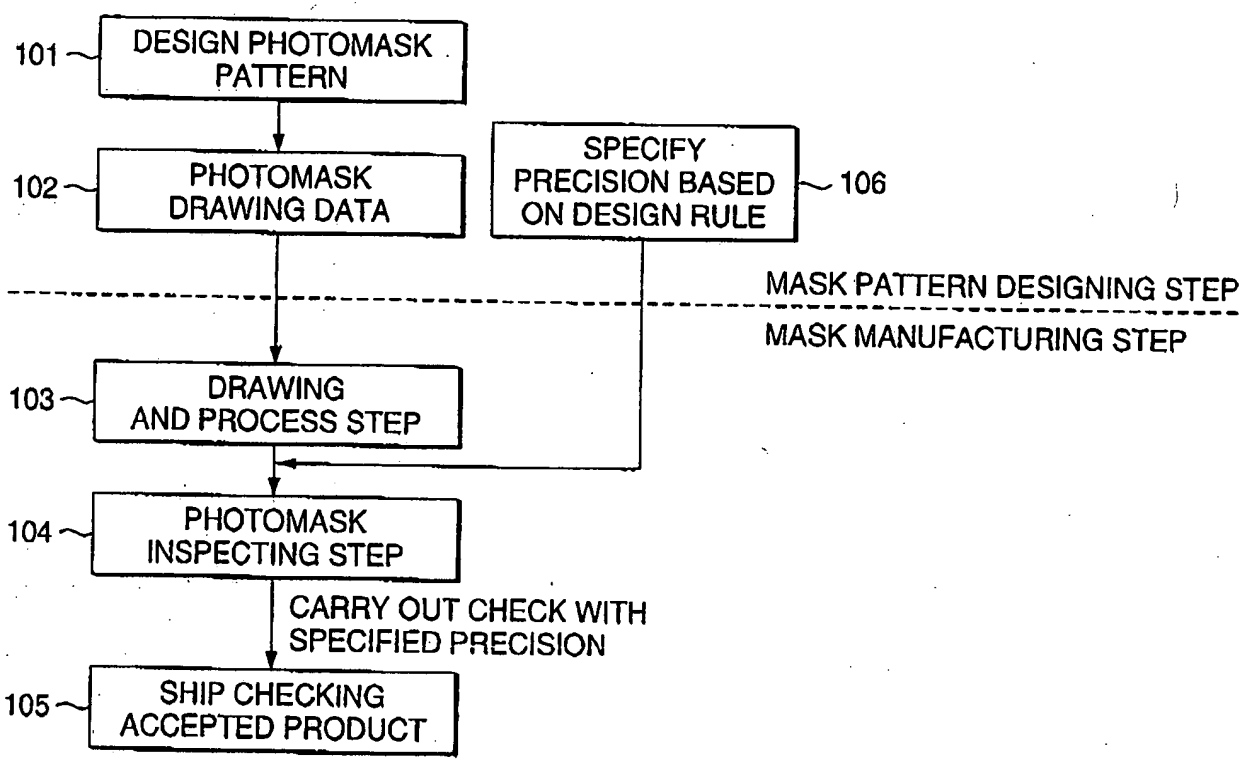

101
DESIGN PHOTOMASK PATTERN
102
PHOTOMASK DRAWING DATA
SPECIFY PRECISION BASED ON DESIGN RULE
106
MASK PATTERN DESIGNING STEP
MASK MANUFACTURING STEP
103
DRAWING AND PROCESS STEP
104
PHOTOMASK INSPECTING STEP
CARRY OUT CHECK WITH SPECIFIED PRECISION
105
SHIP CHECKING ACCEPTED PRODUCT

FIG. 26B

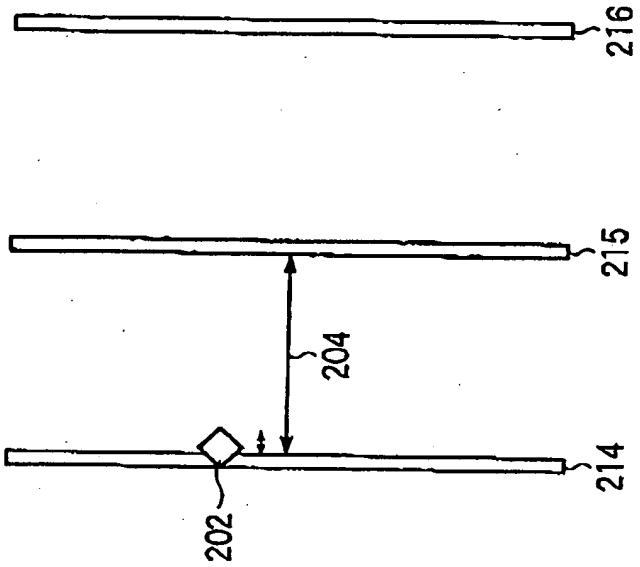


FIG. 26A